

# CONGESTION-FREE SWITCH SYSTEM

Fig 1A

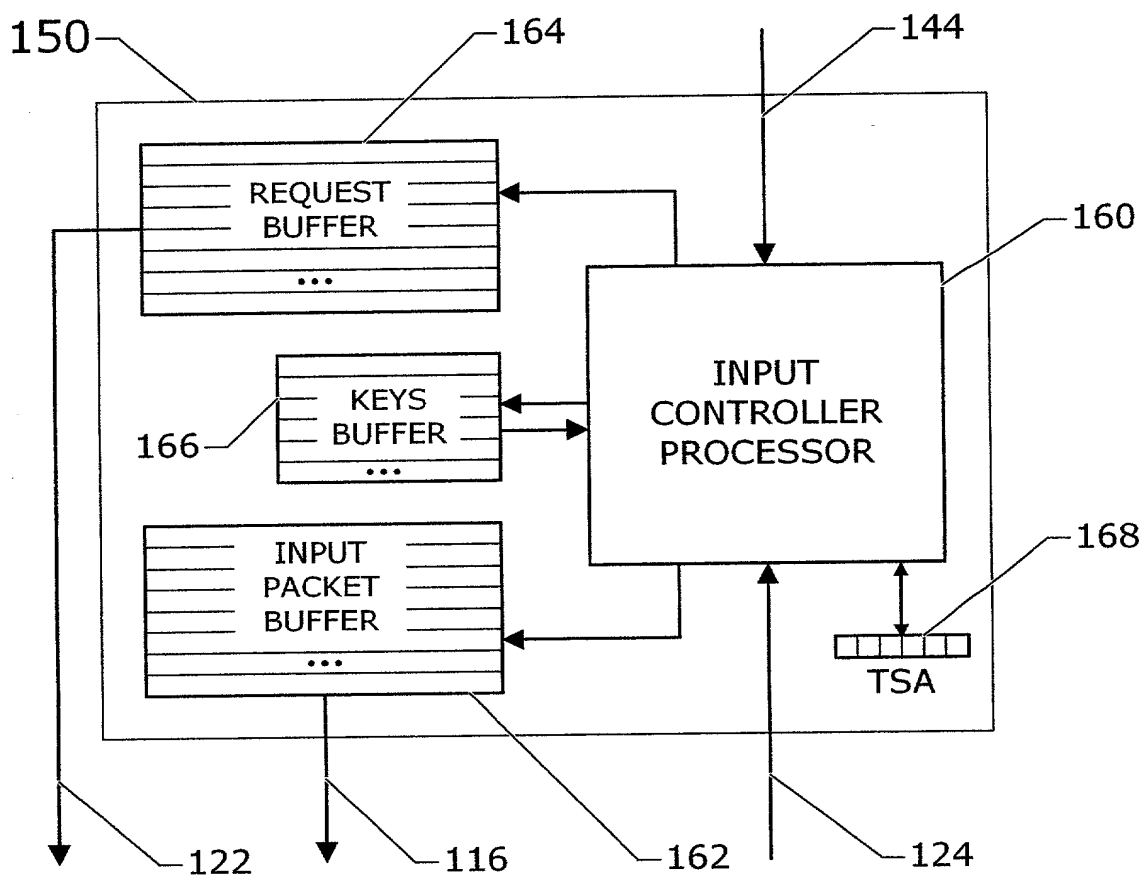


Fig 1B

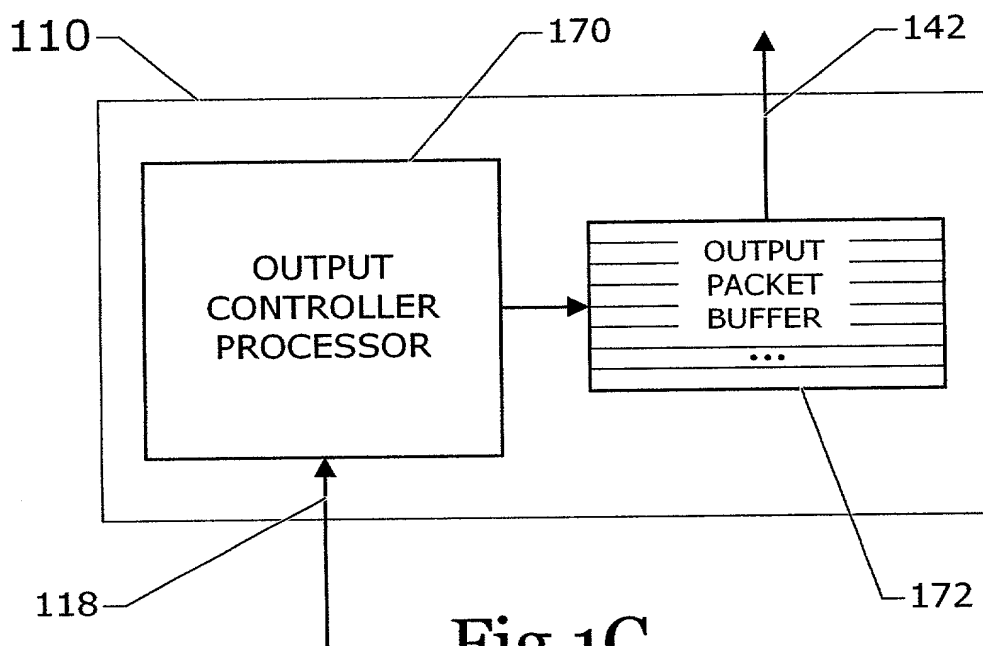
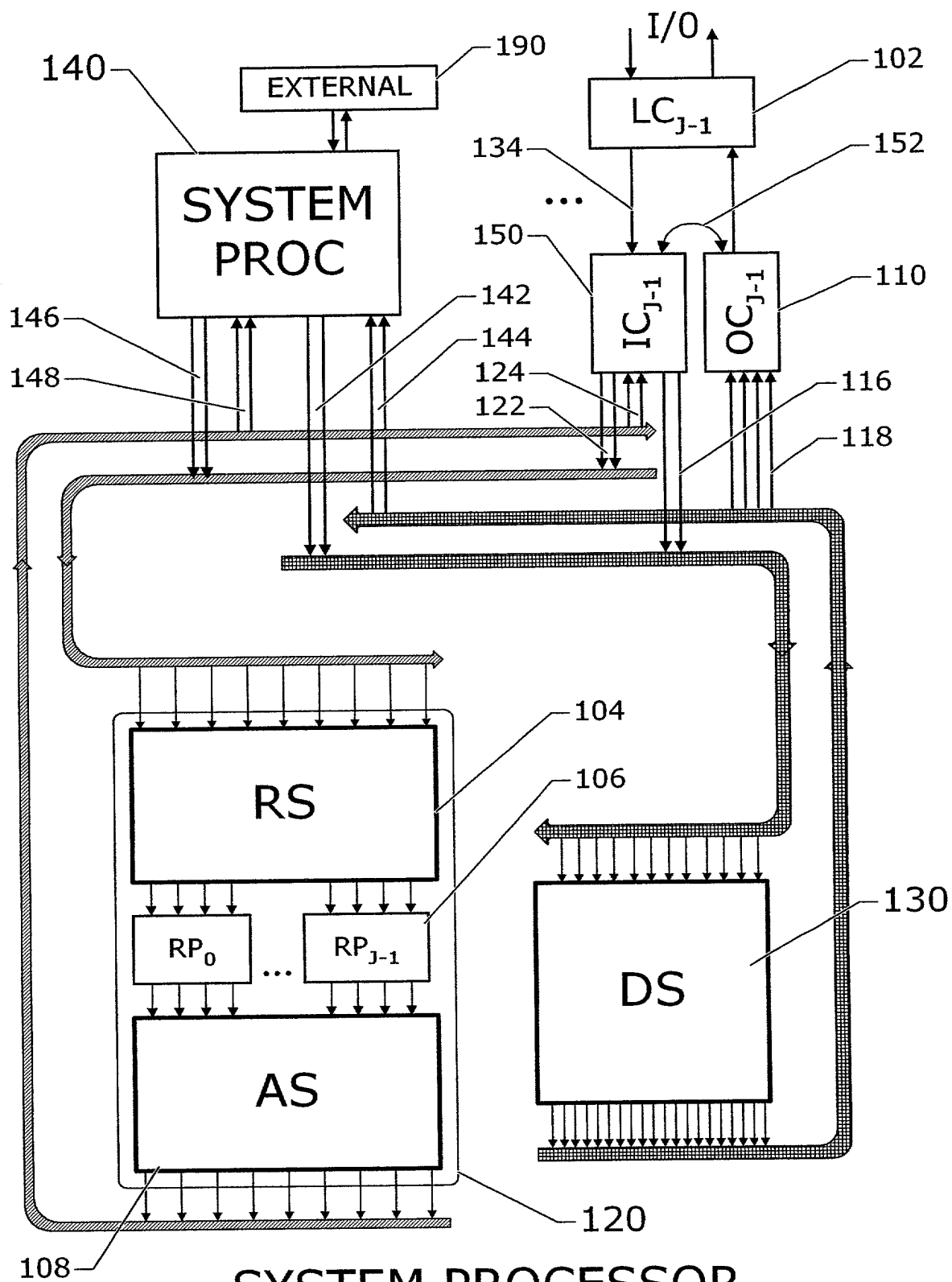


Fig 1C

# INPUT AND OUTPUT CONTROLLERS



SYSTEM PROCESSOR

Fig 1D

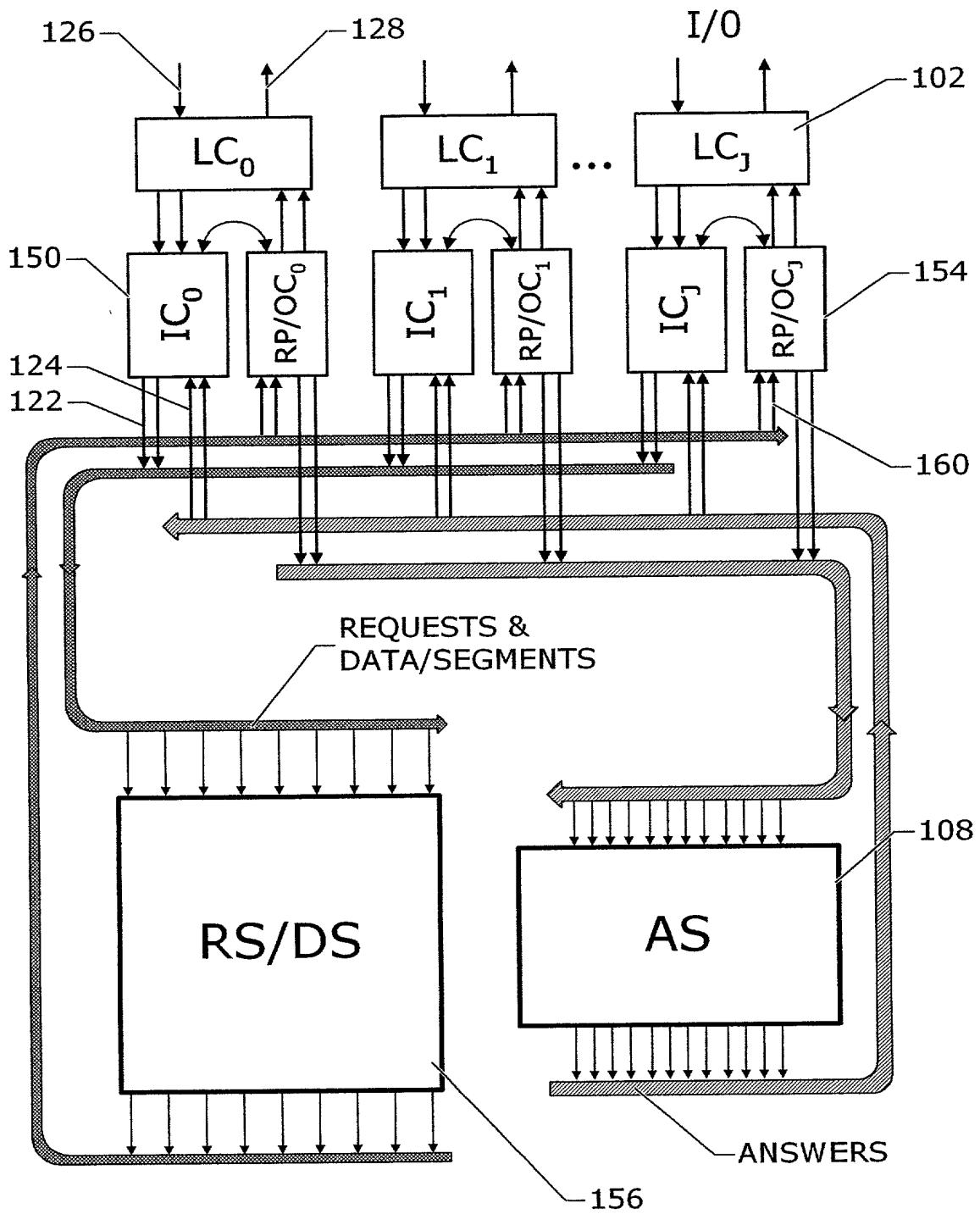


Fig 1E

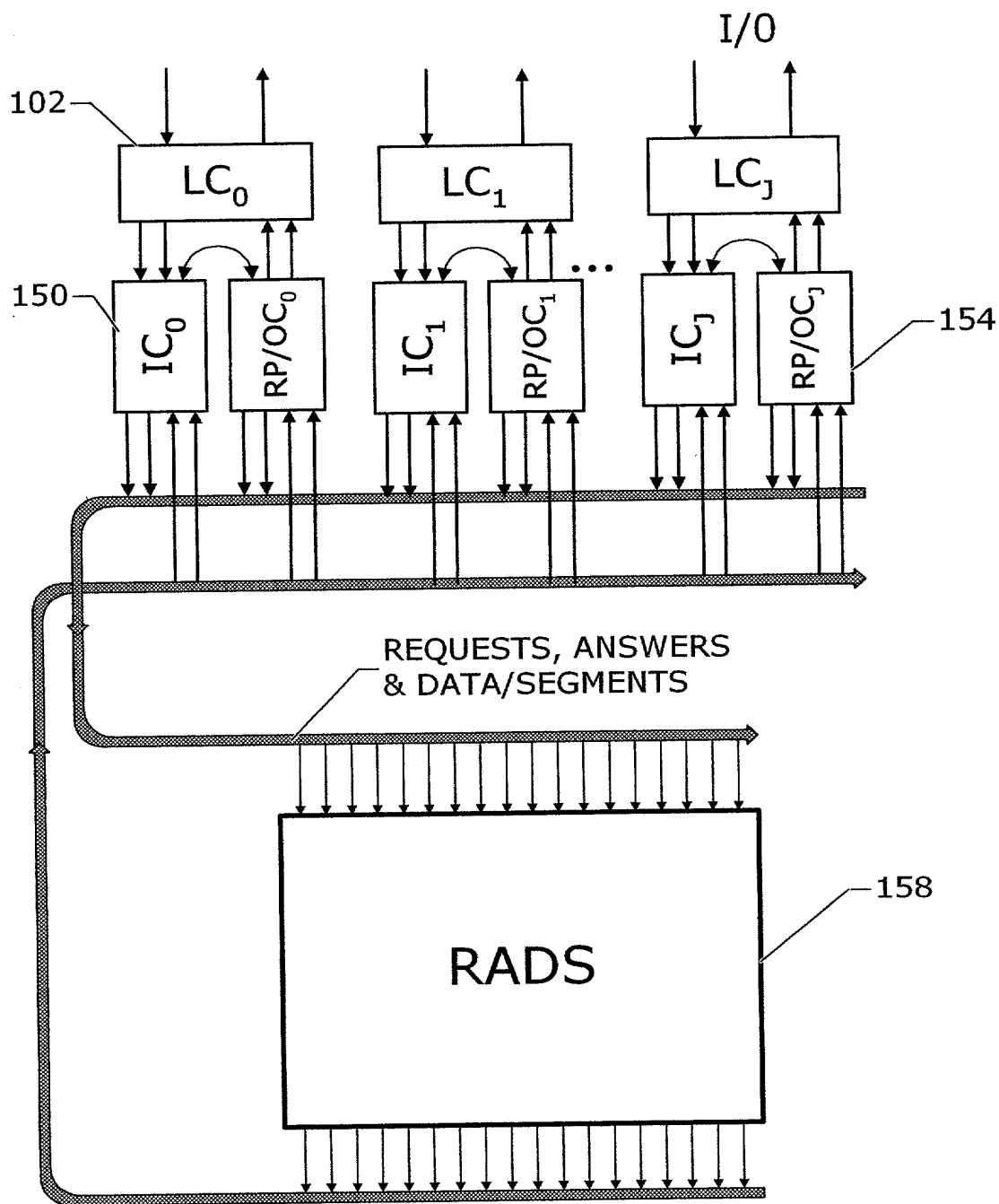
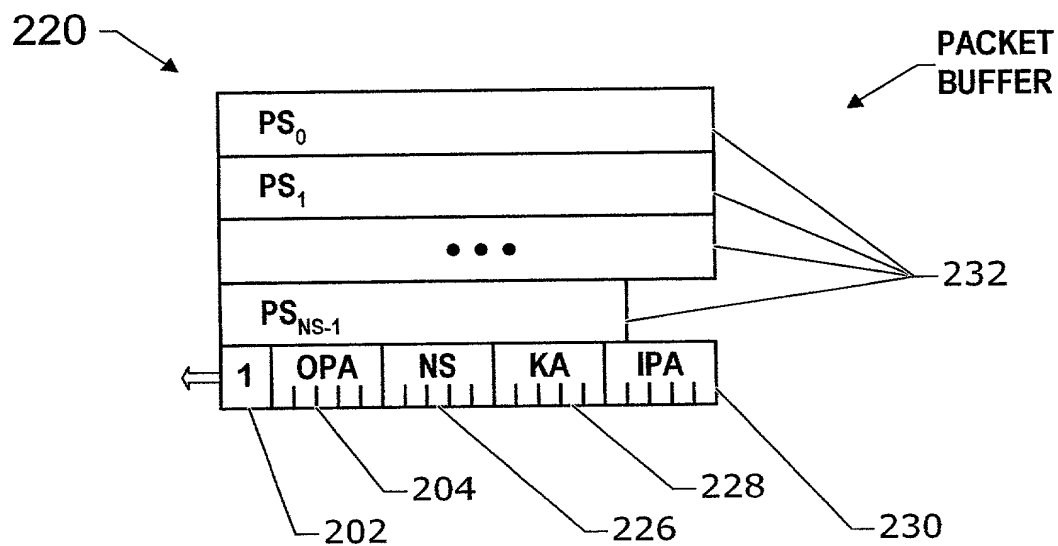
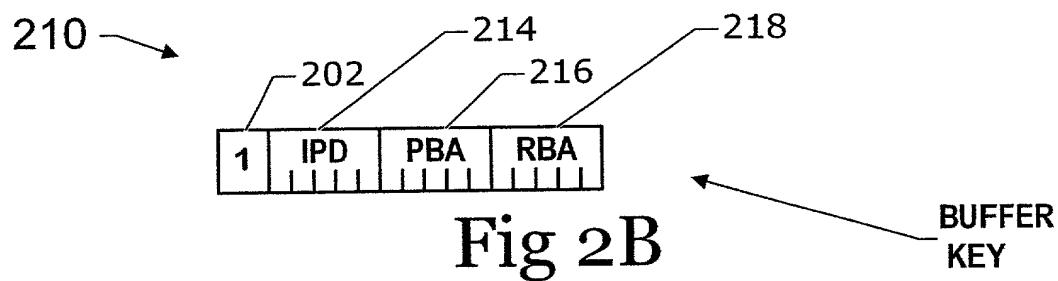
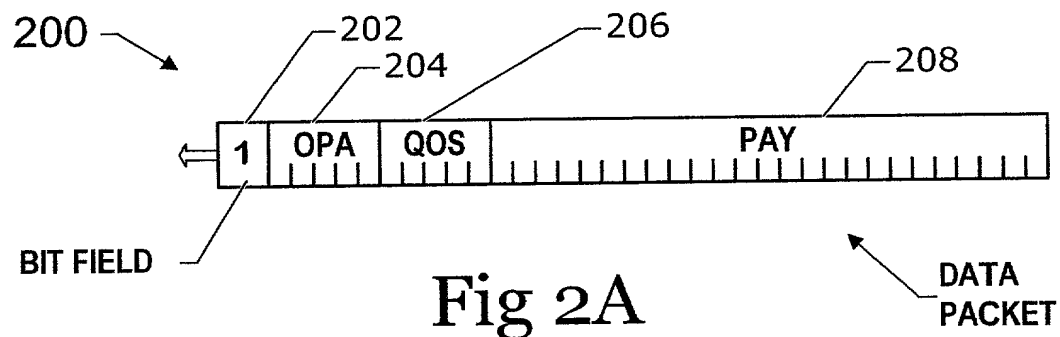


Fig 1F



**Fig 2C**

PACKET FORMATS AND LAYOUTS

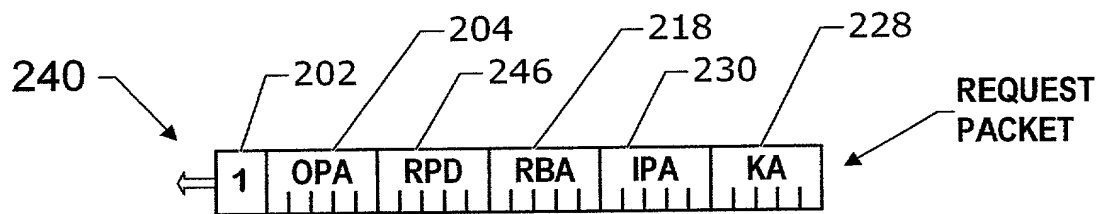


Fig 2D

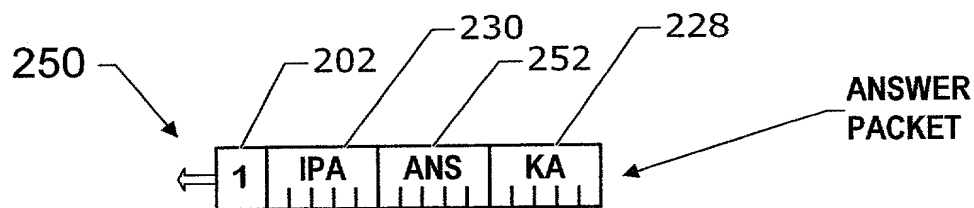


Fig 2E

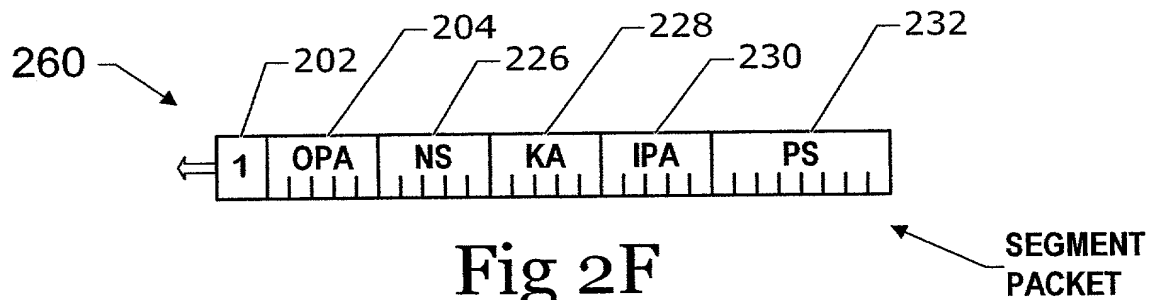
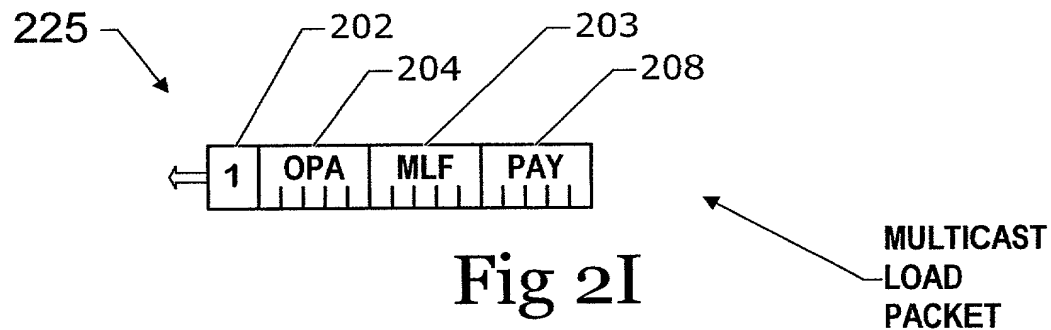
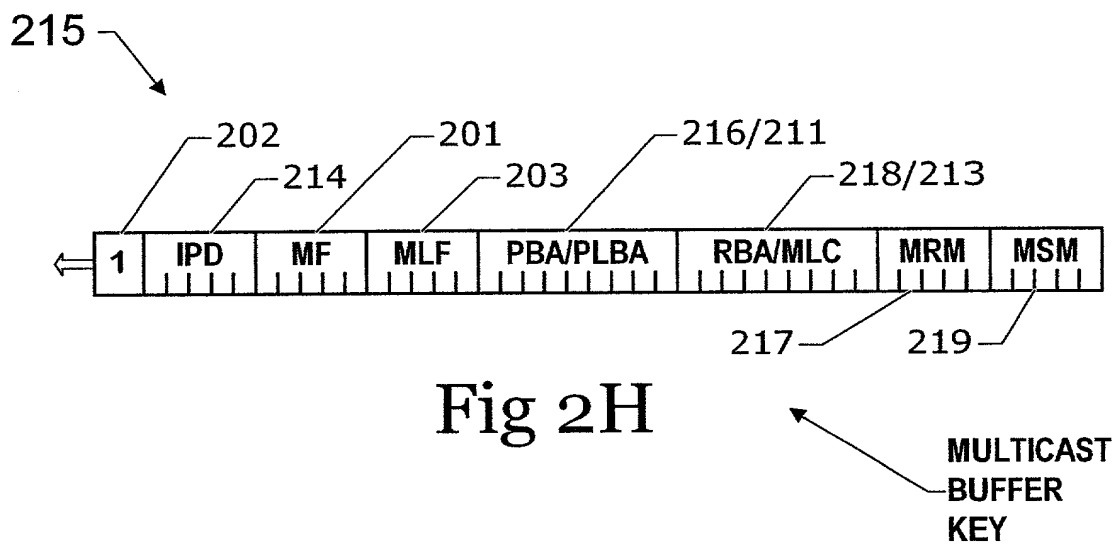
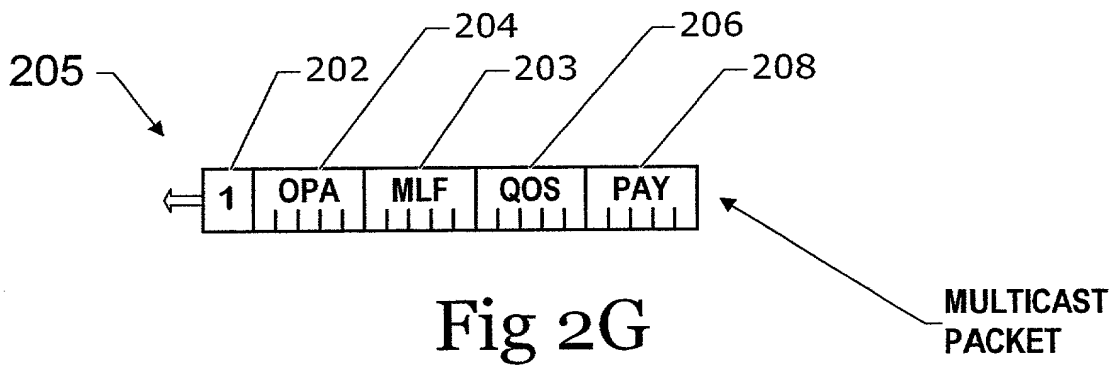


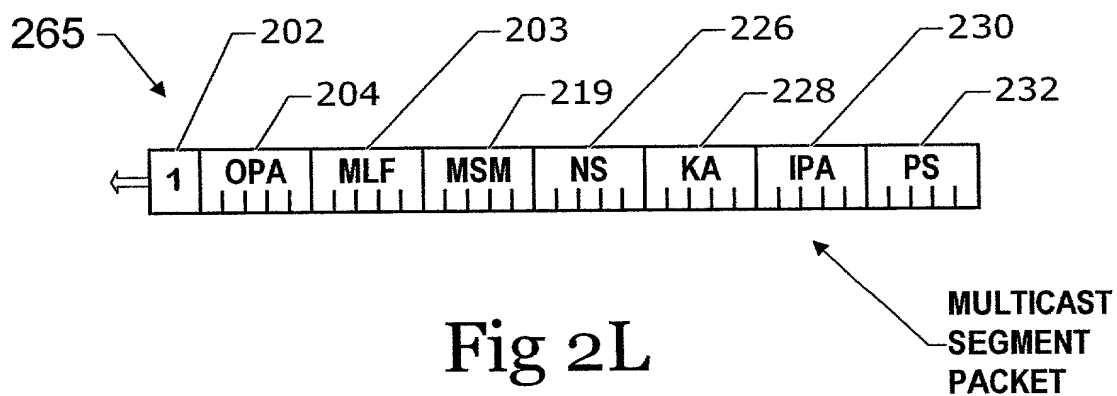
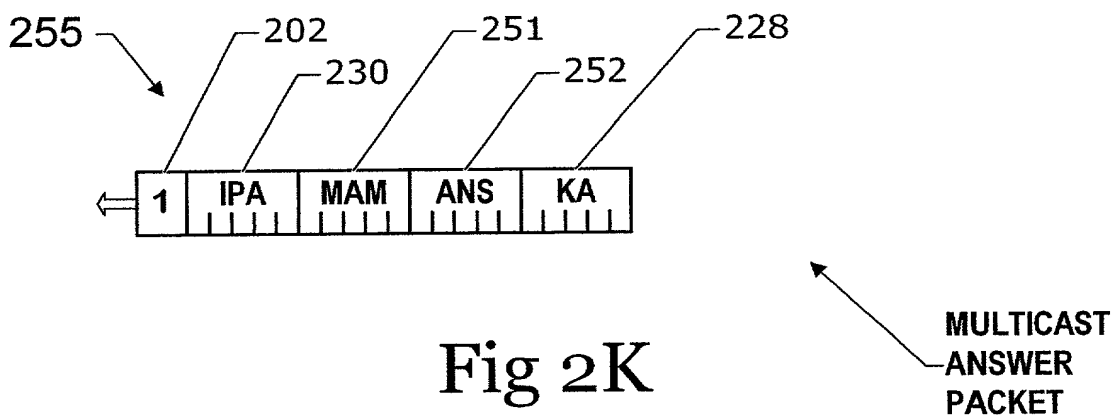
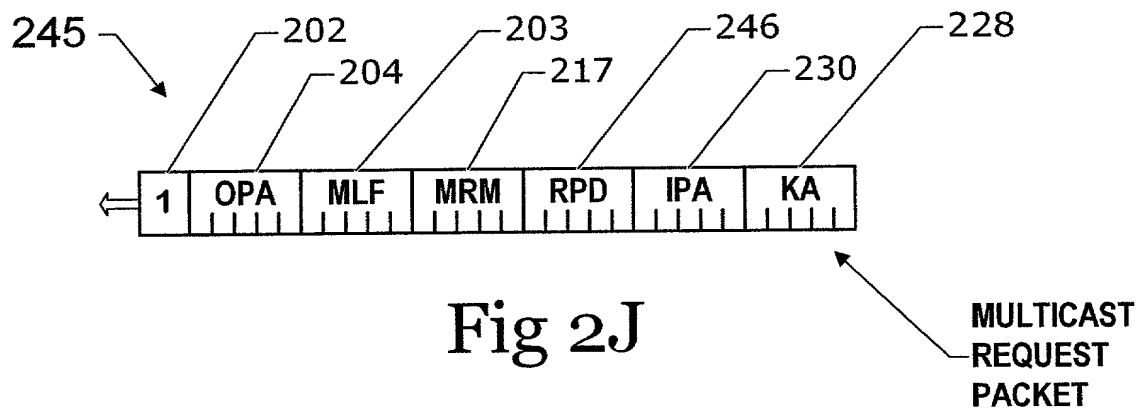
Fig 2F

PACKET FORMATS AND LAYOUTS



## PACKET FORMATS AND LAYOUTS





PACKET FORMATS AND LAYOUTS

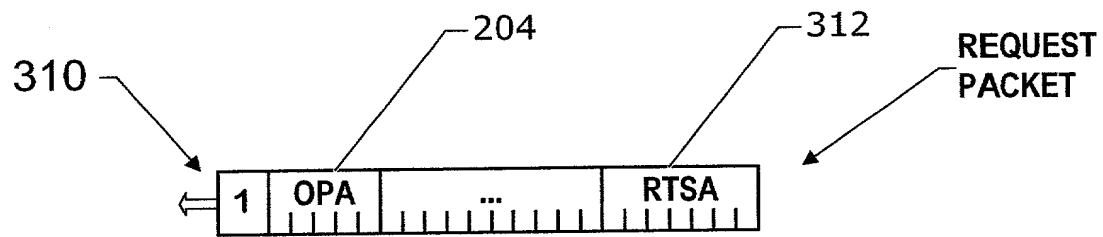


Fig 3A

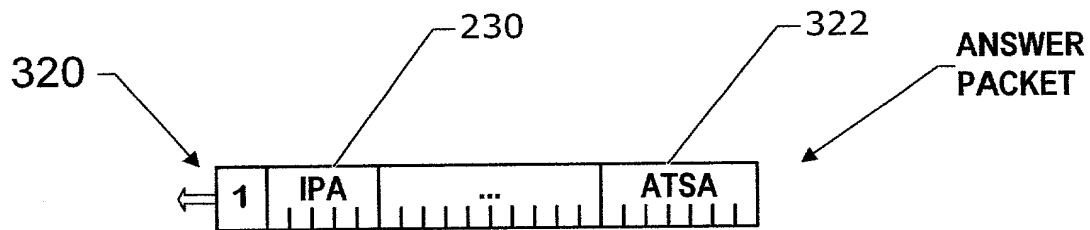
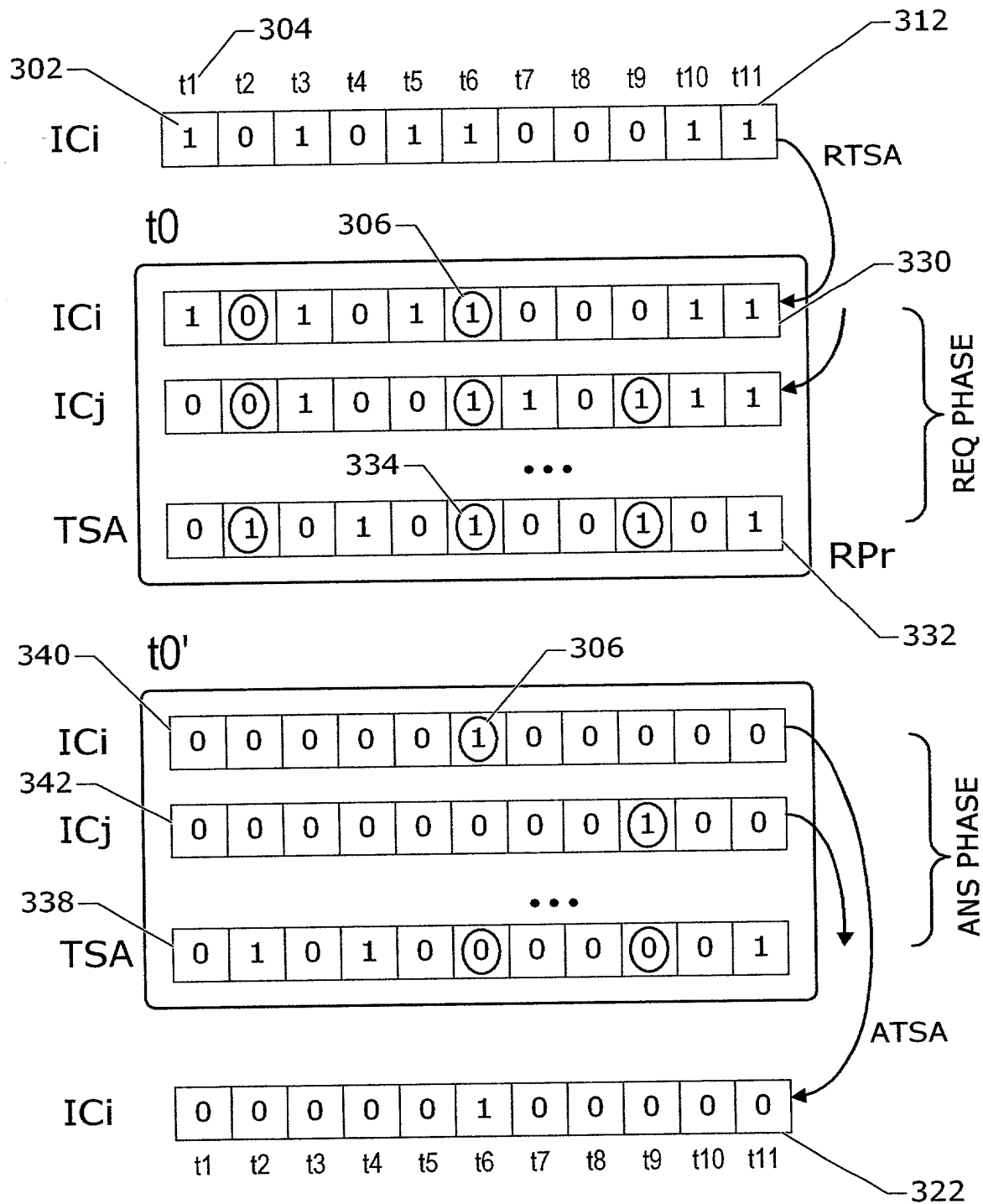


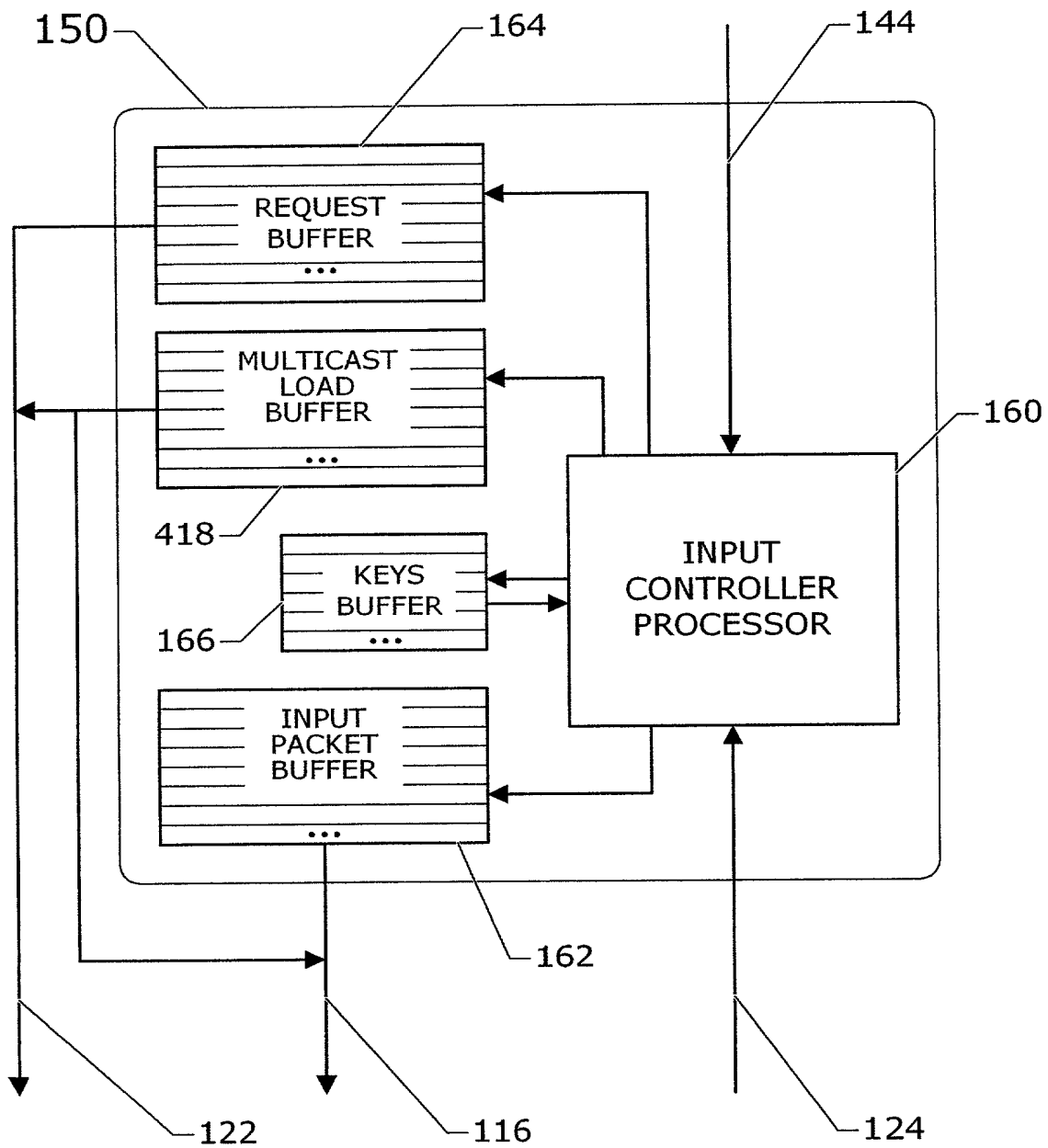
Fig 3B

PACKET FORMATS AND LAYOUTS



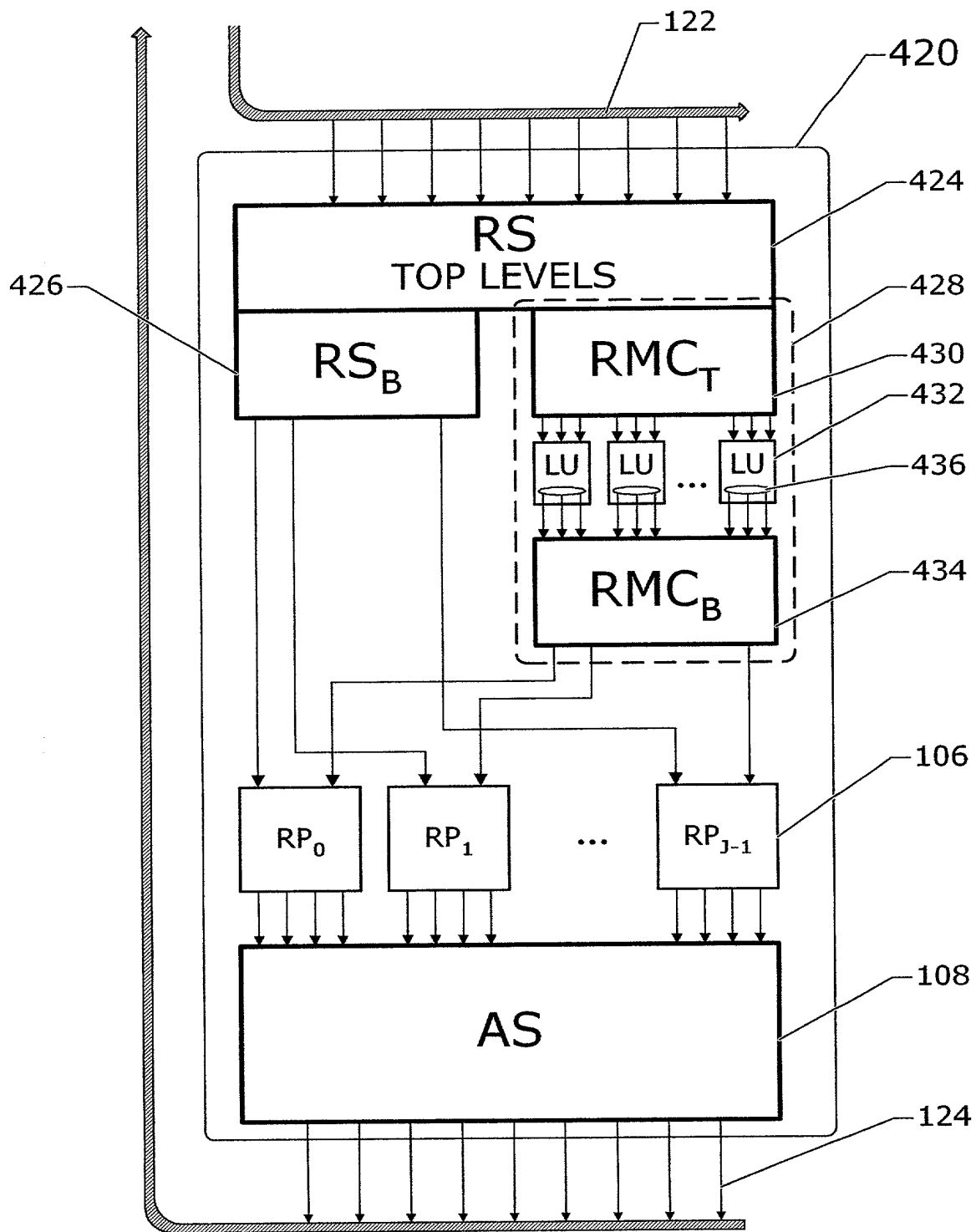
TIME-SLOT RESERVATION

Fig 3C



MULTICAST INPUT CONTROLLER

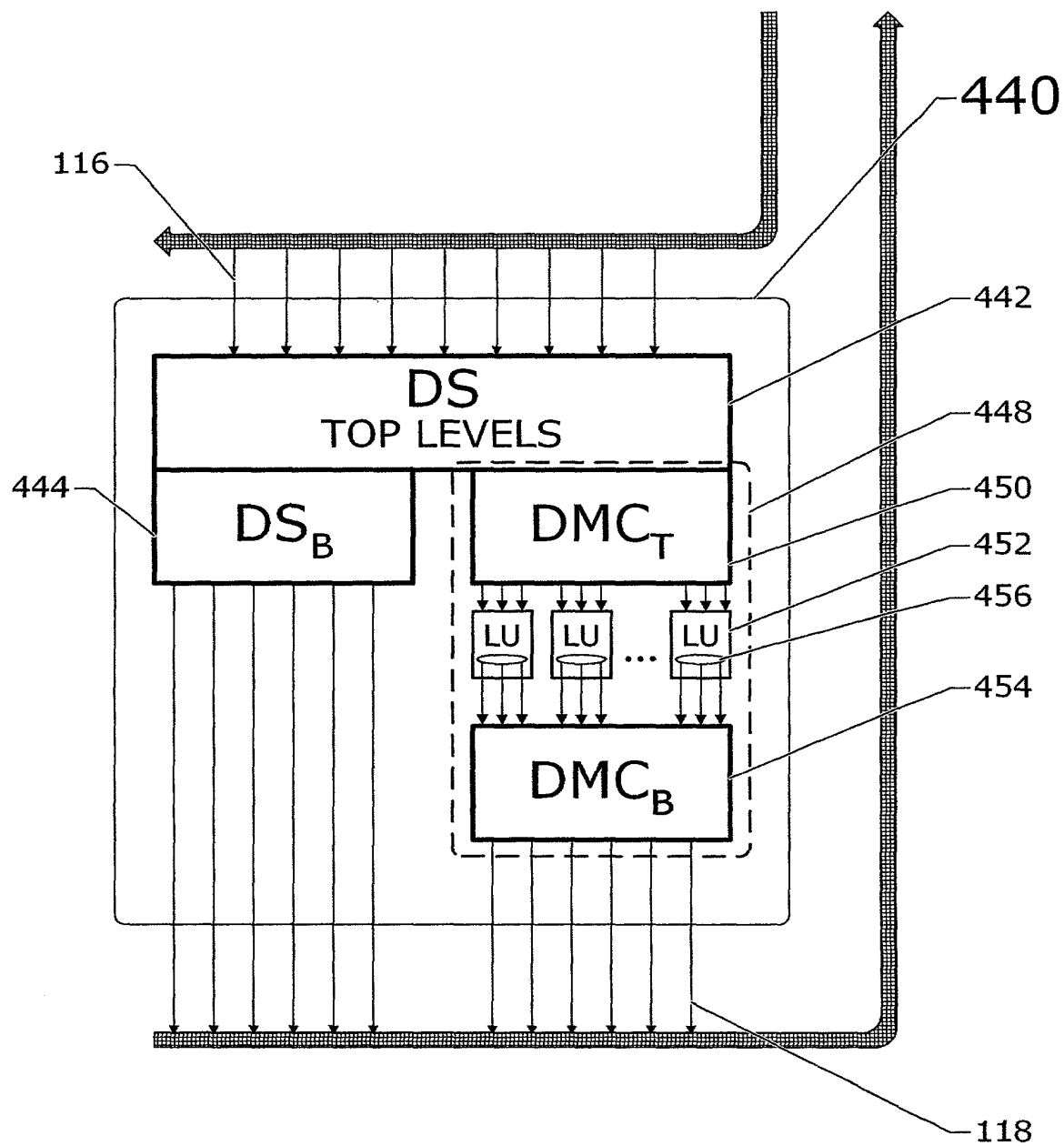
Fig 4A



MULTICAST CONTROL SYSTEM

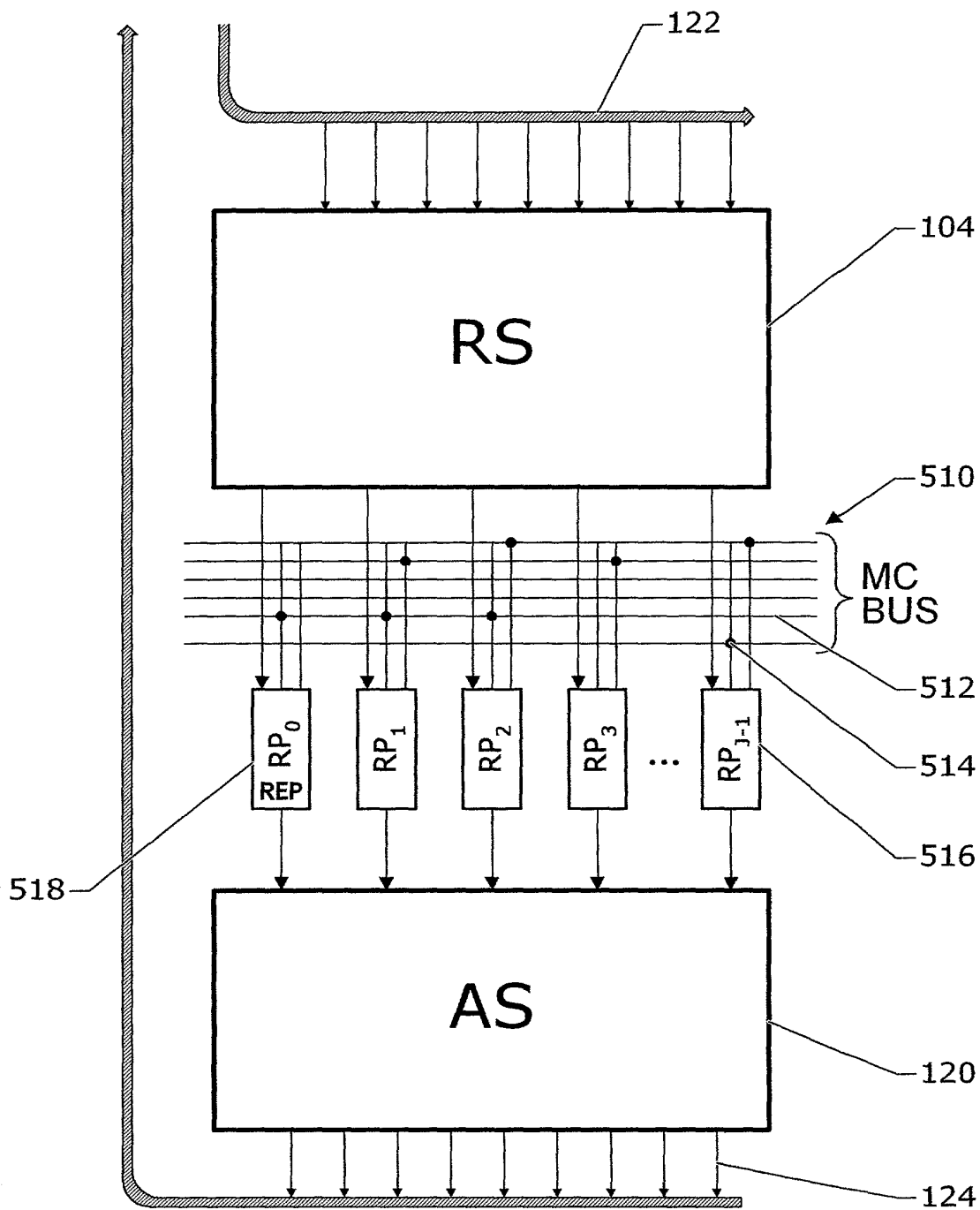
Fig 4B

TOP SECRET



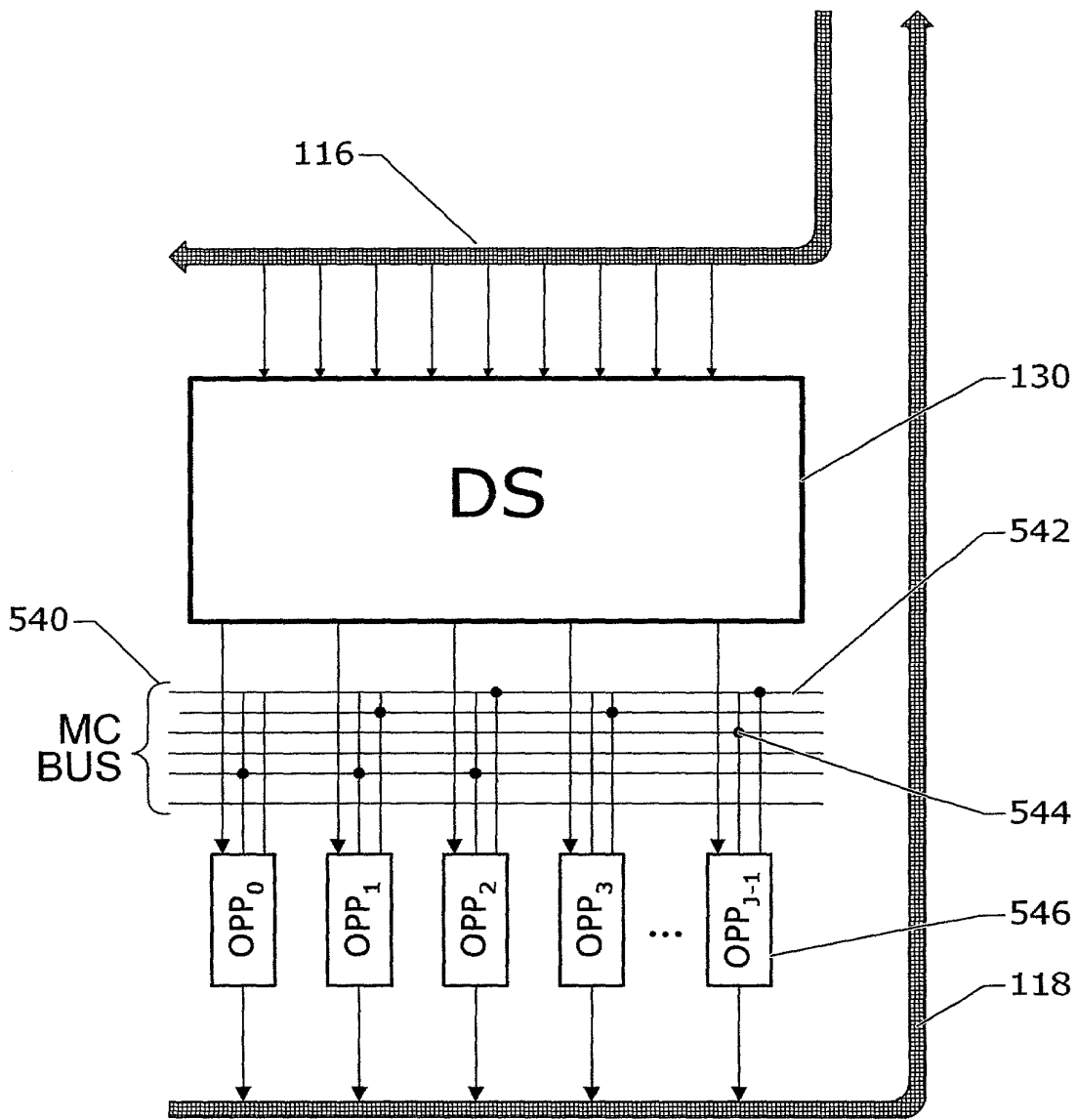
MULTICAST DATA SWITCH

Fig 4C



MULTICAST BUS CONTROL SYSTEM

Fig 5A



MULTICAST BUS DATA SWITCH

Fig 5B



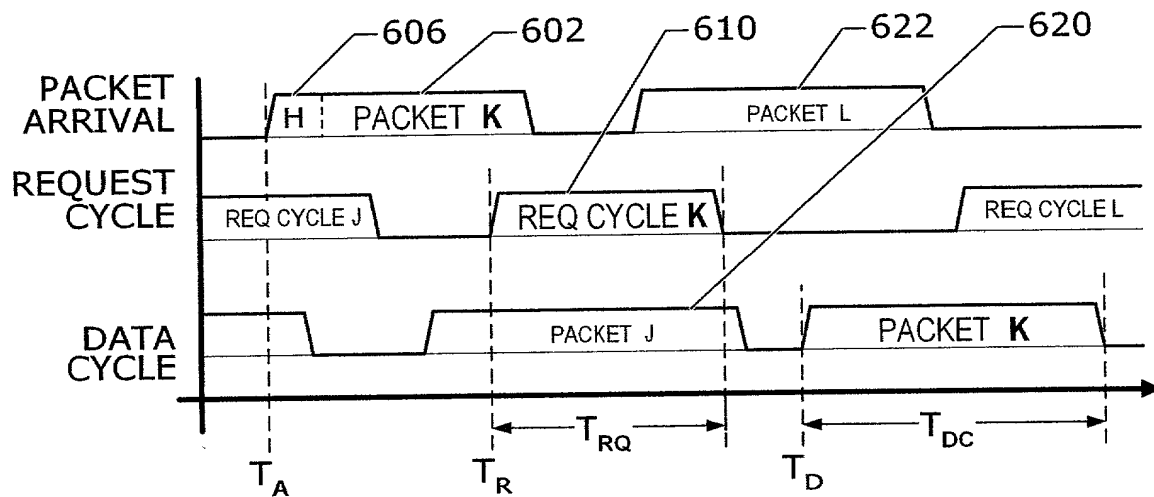


Fig 6A

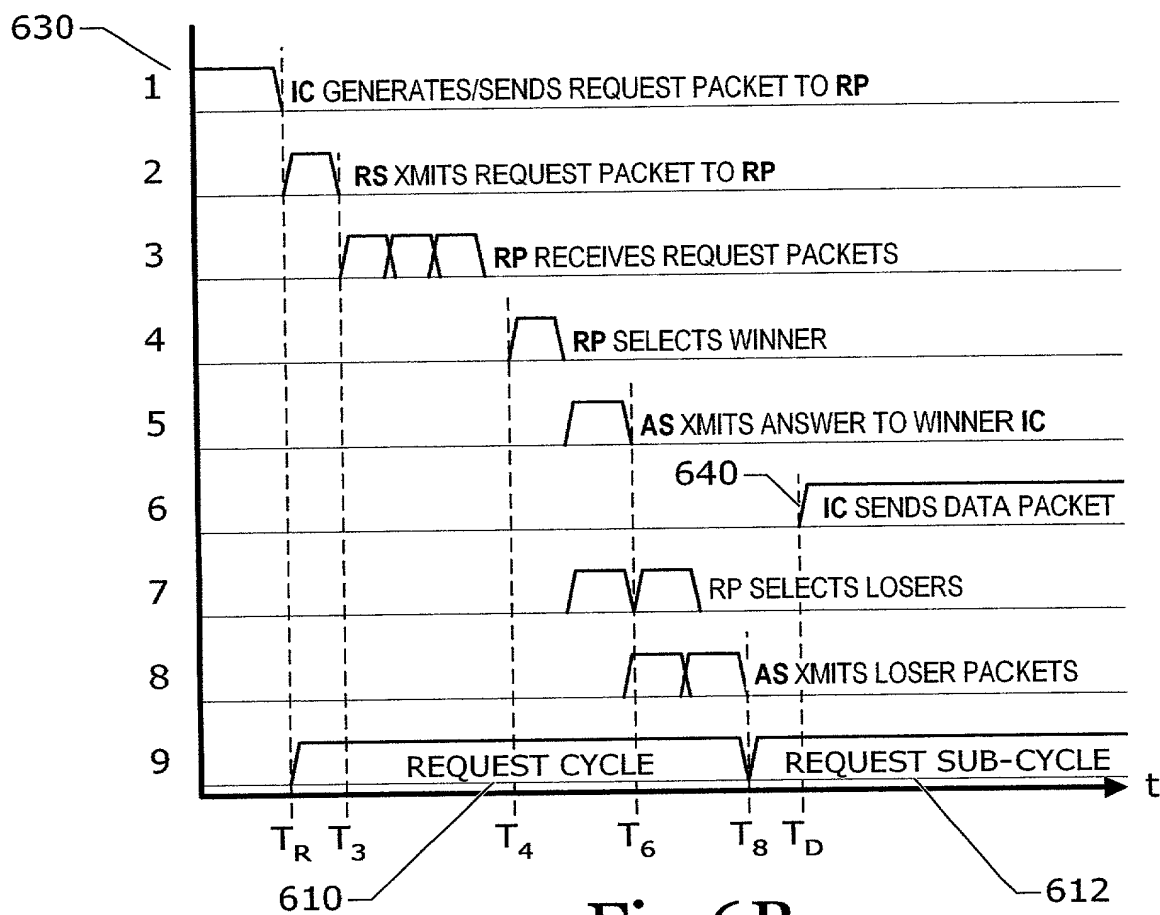


Fig 6B

CONTROL AND DATA CYCLE TIMING

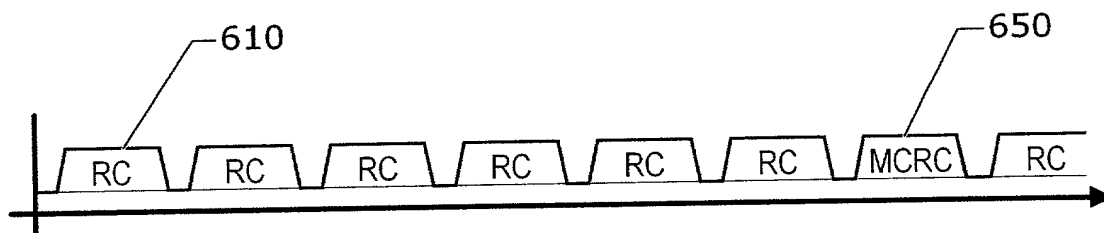


Fig 6C

# MULTICAST CONTROL CYCLE TIMING

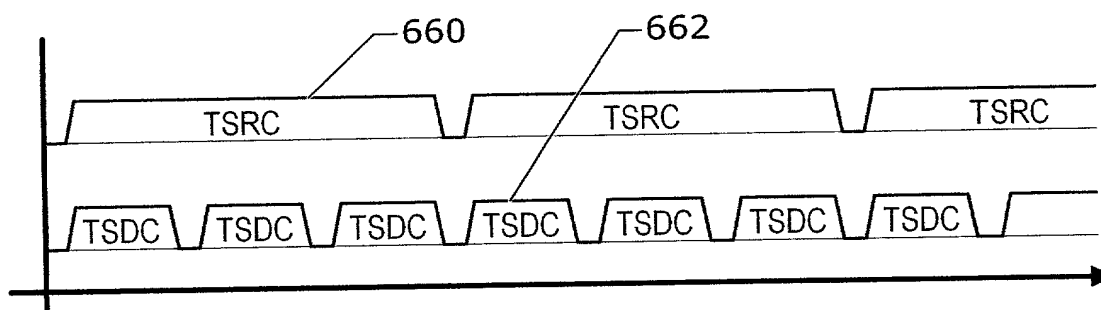


Fig 6D

# TIME-SLOT RESERVATION TIMING

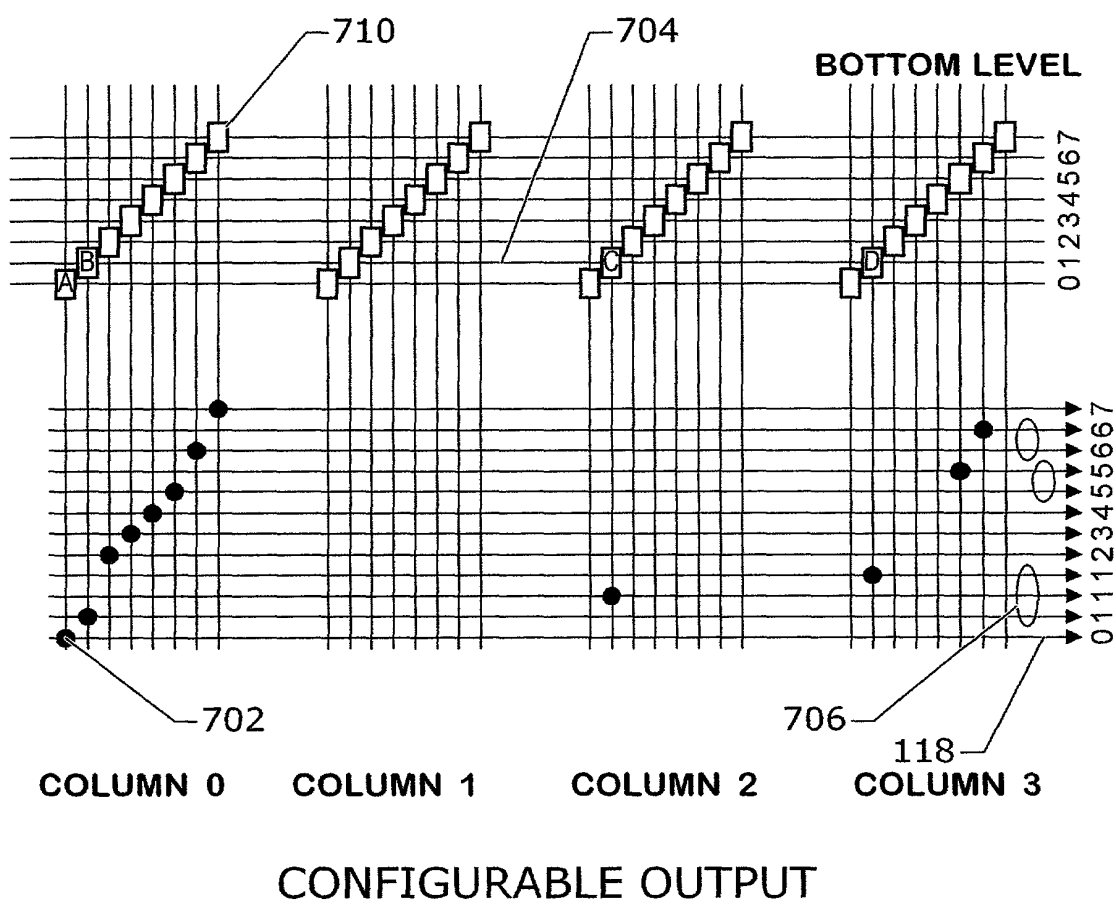
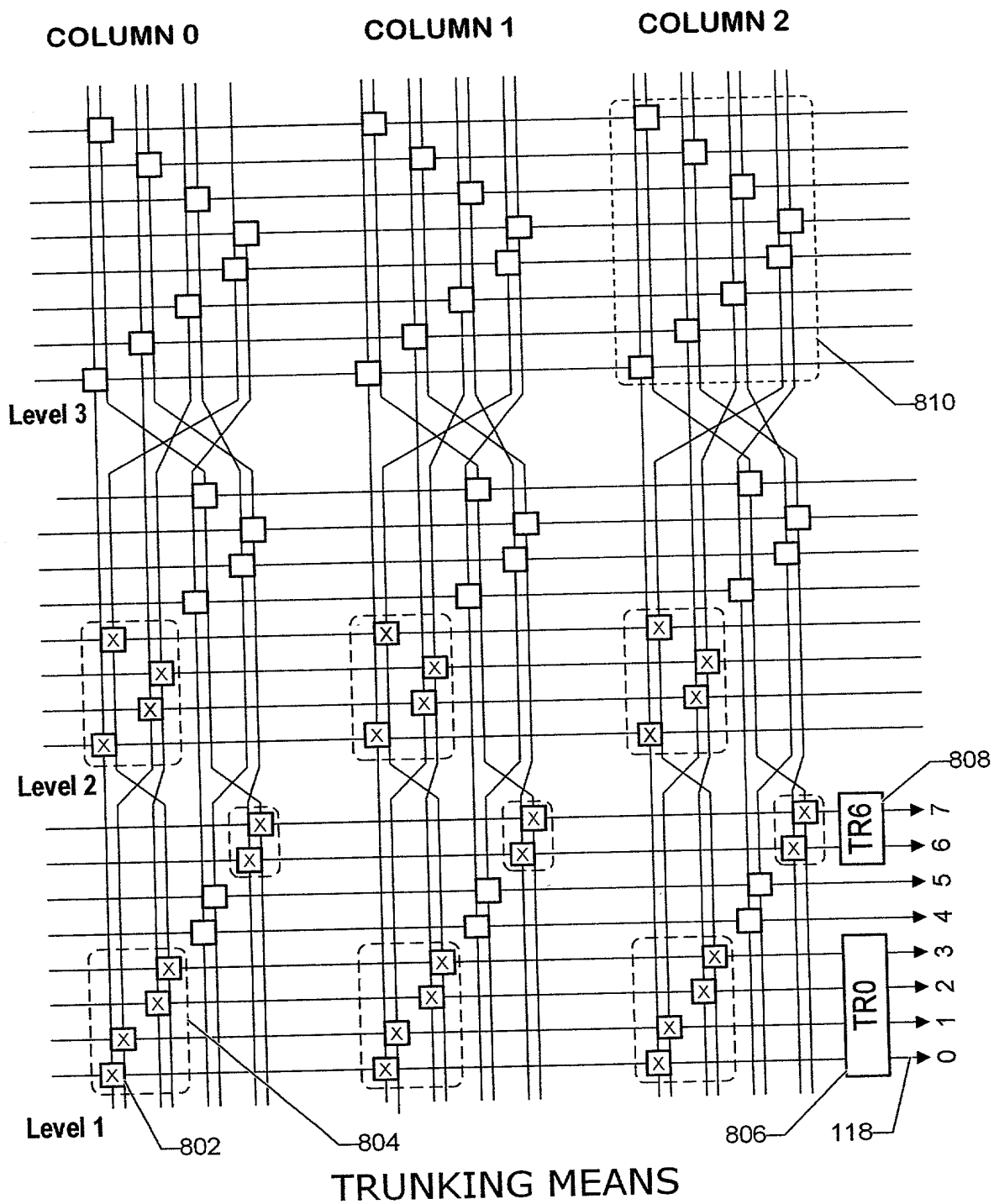
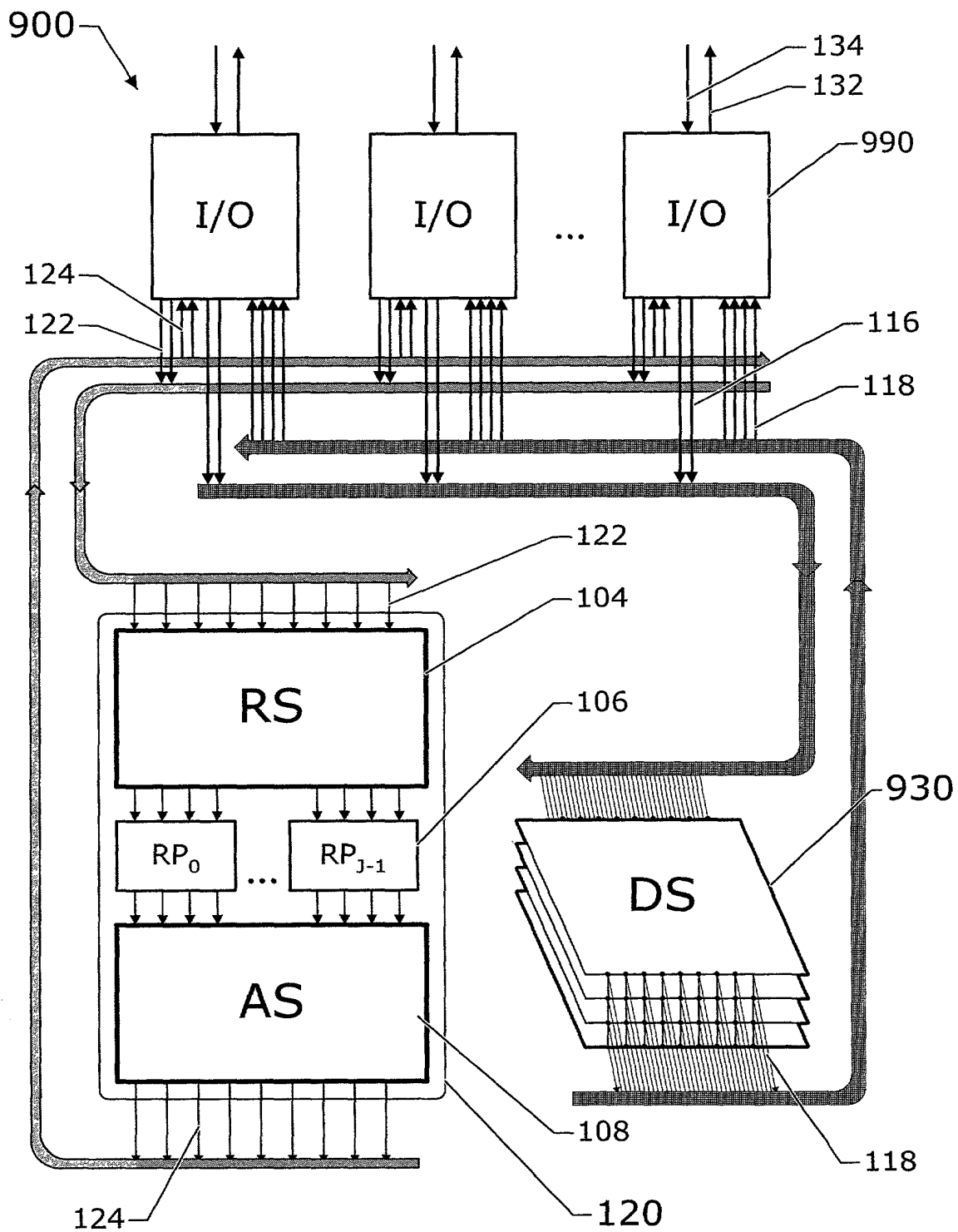


Fig 7



**Fig 8**



PARALLEL DATA SWITCH

Fig 9

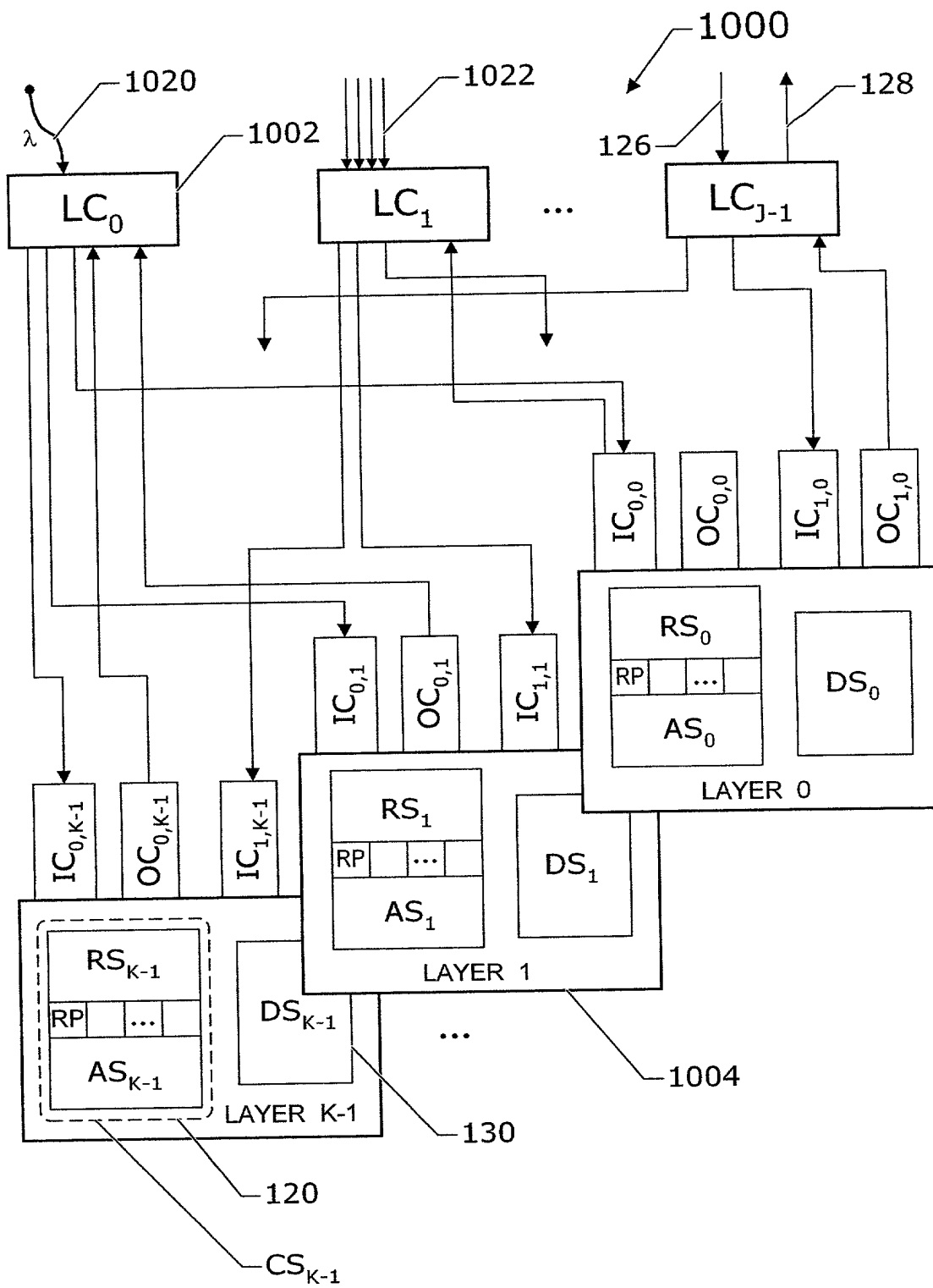


Fig 10A

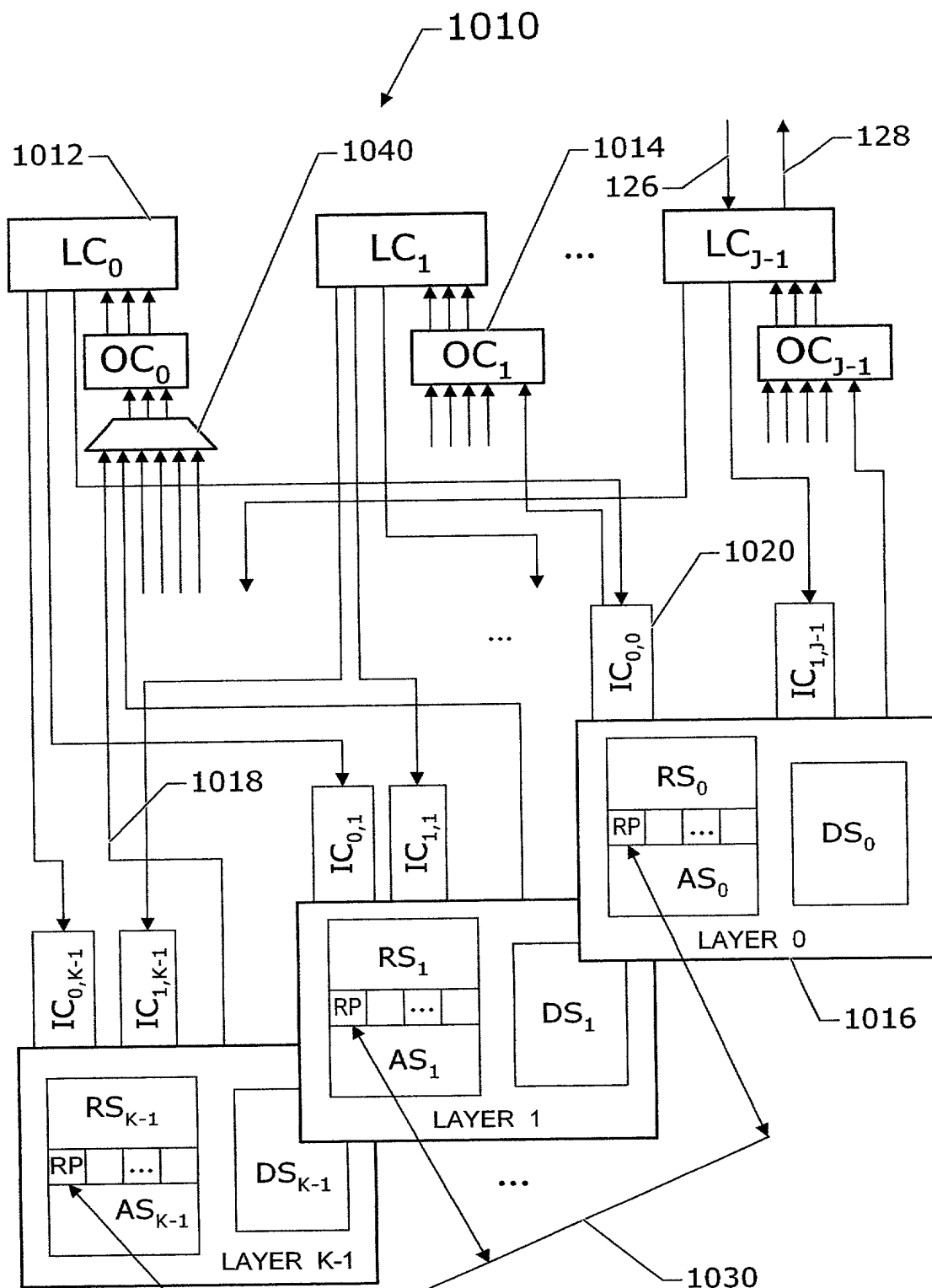
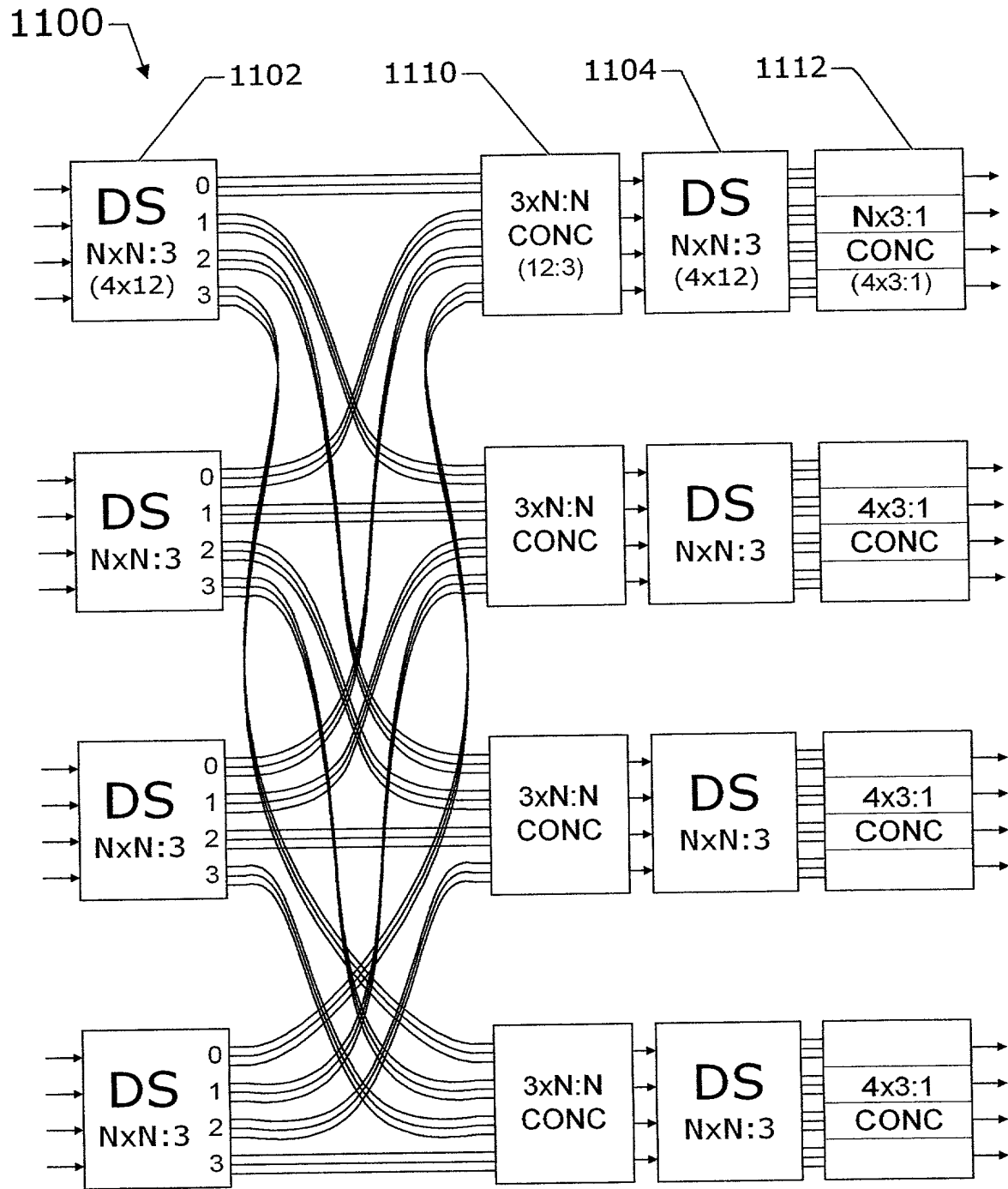


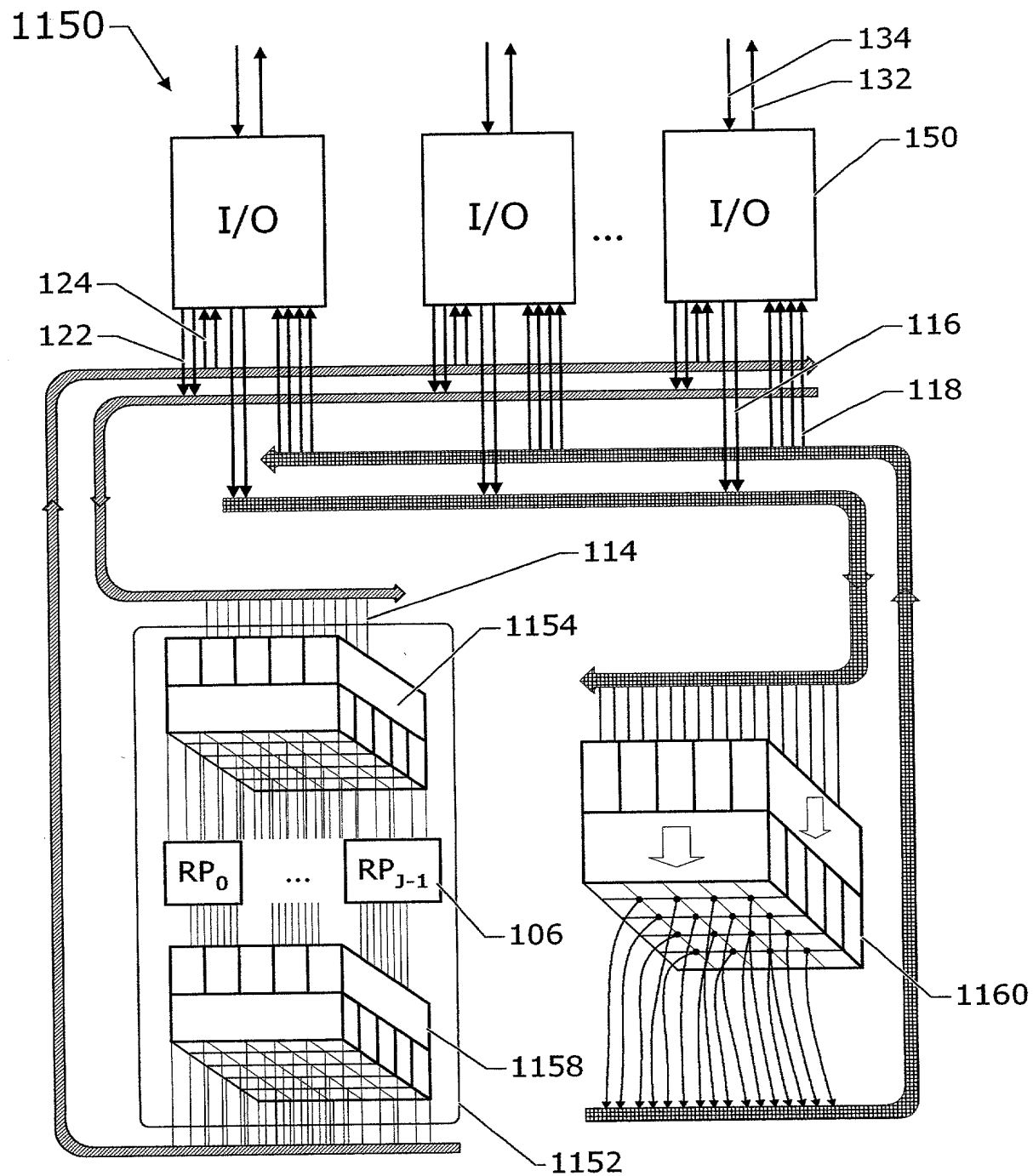
Fig 10B



TWISTED CUBE DATA SWITCH

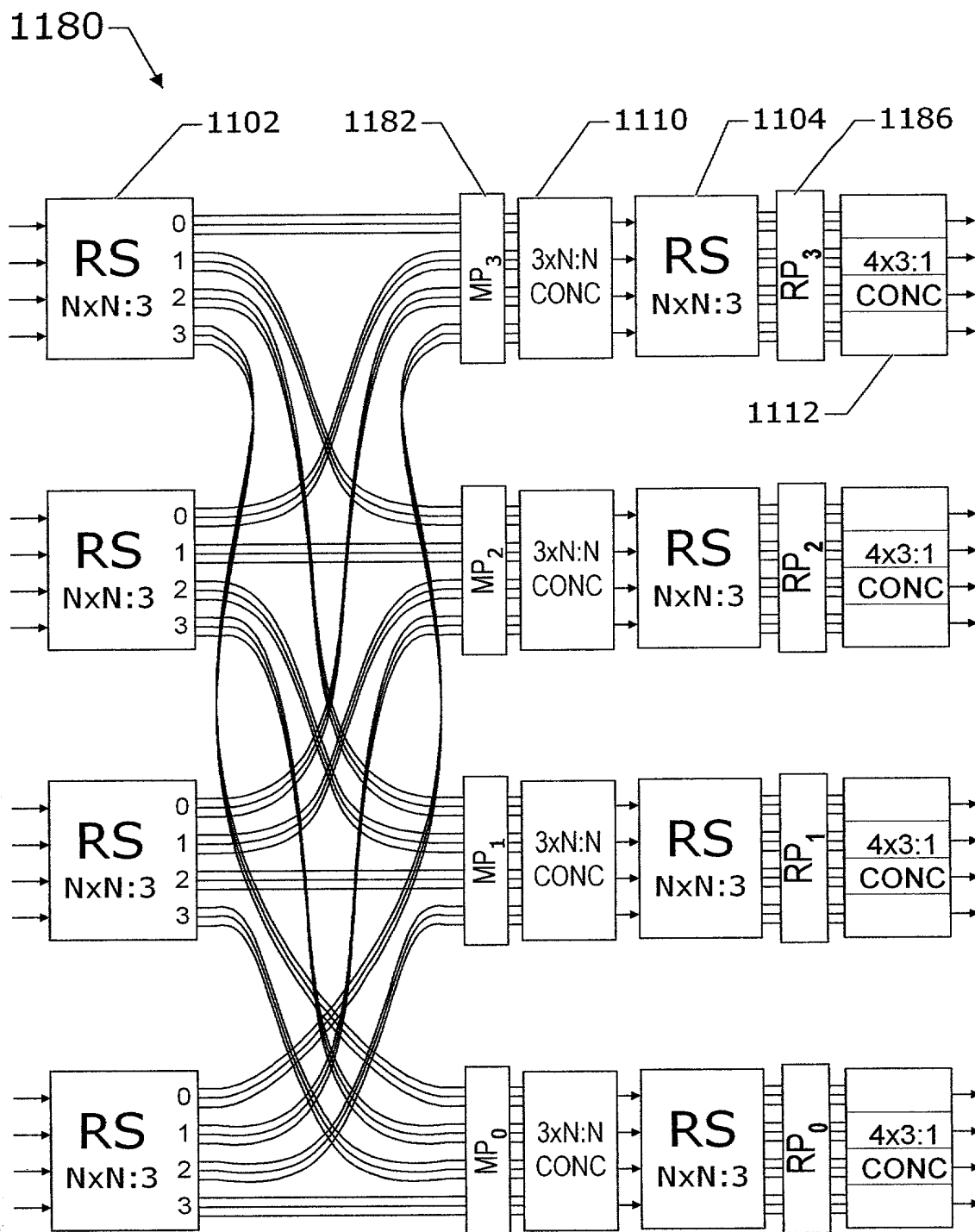
Fig 11A





TWISTED CUBE CONTROL & DATA SWITCHES

Fig 11B



TWISTED CUBE CONTROL

Fig 11C

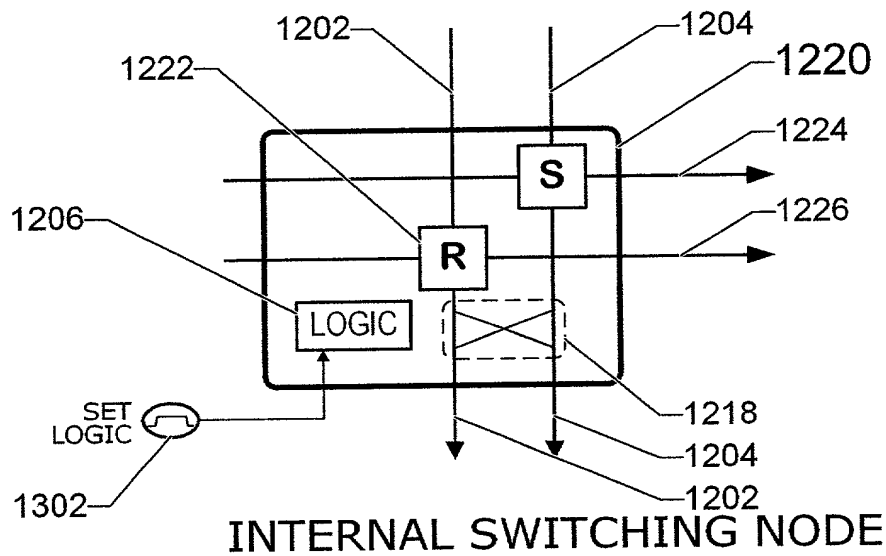


Fig 12A

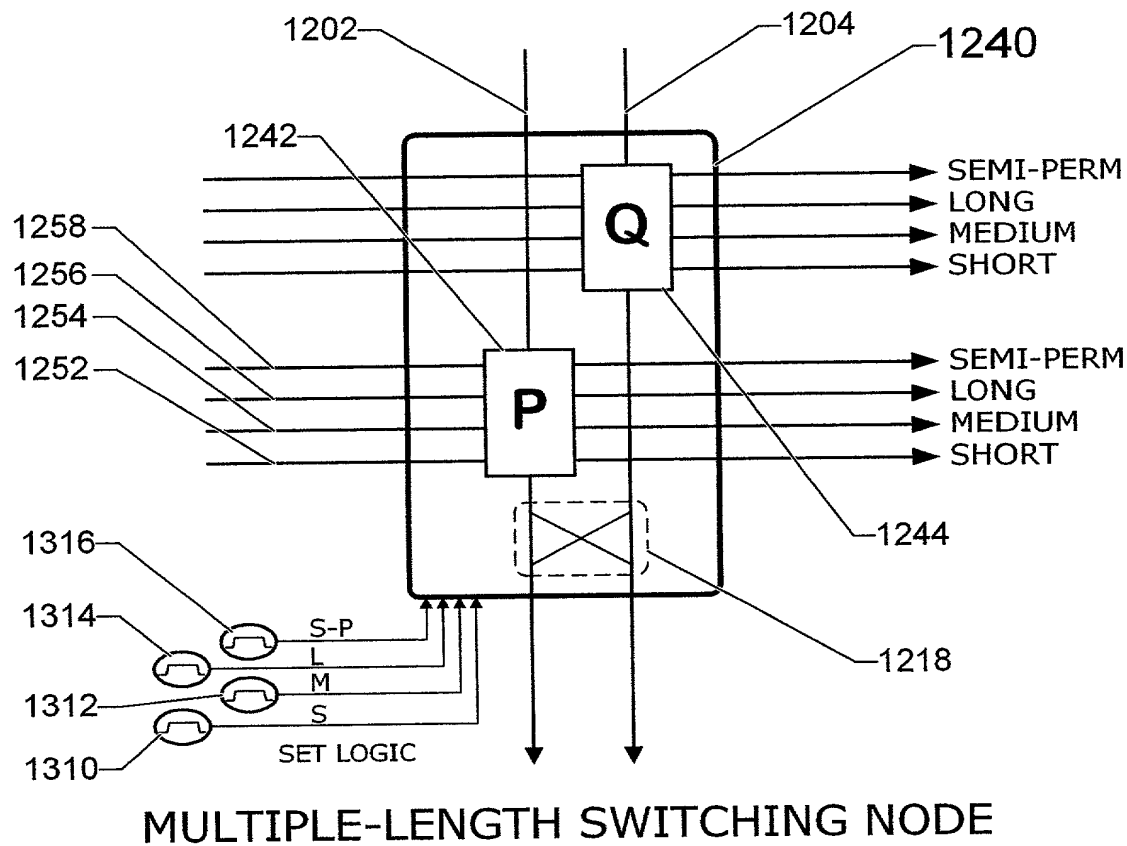


Fig 12B

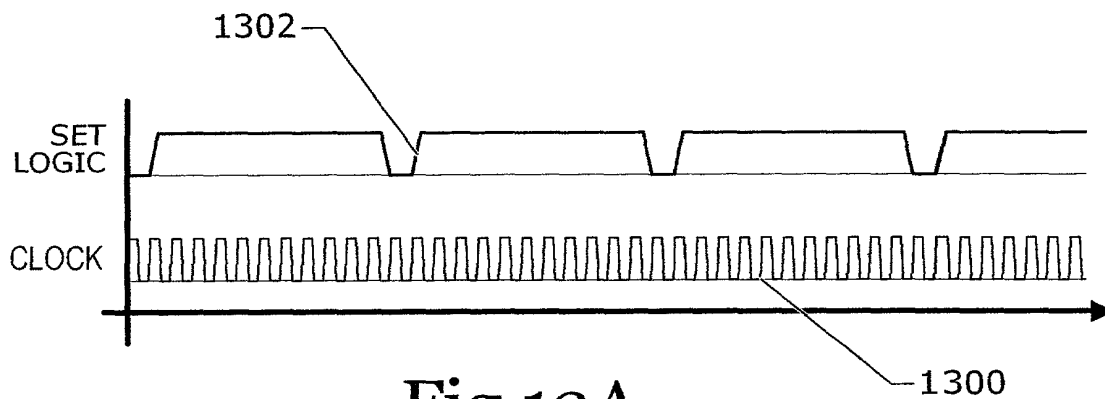


Fig 13A

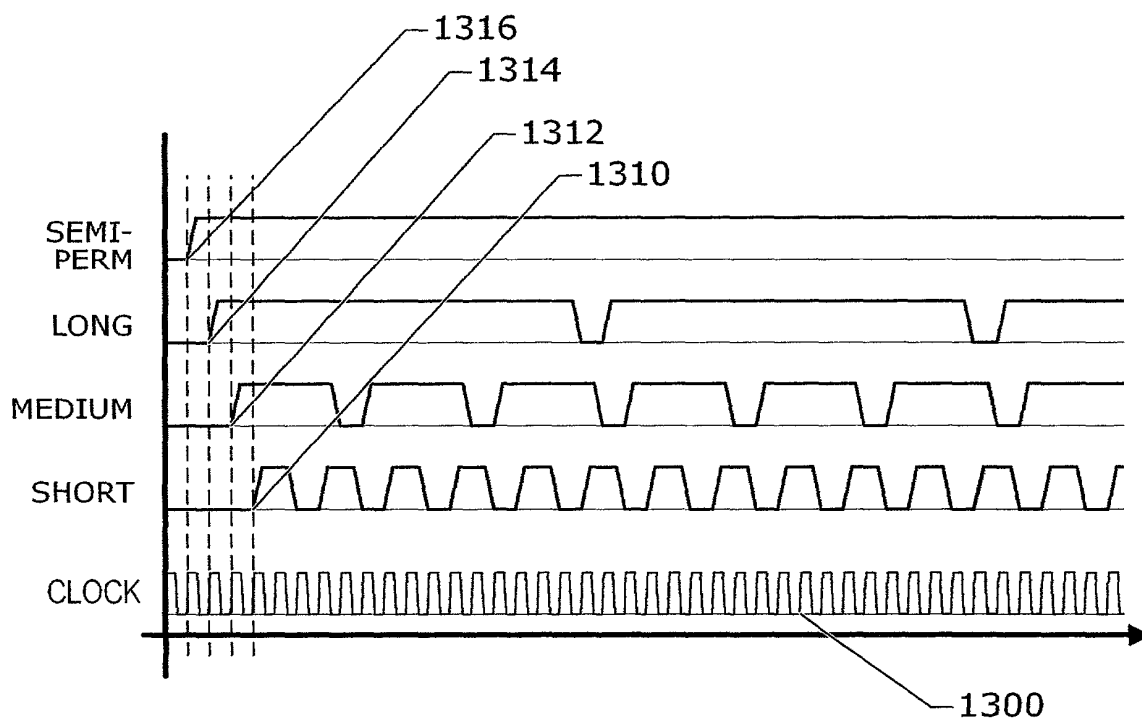


Fig 13B

MULTIPLE-LENGTH SWITCHING TIMING

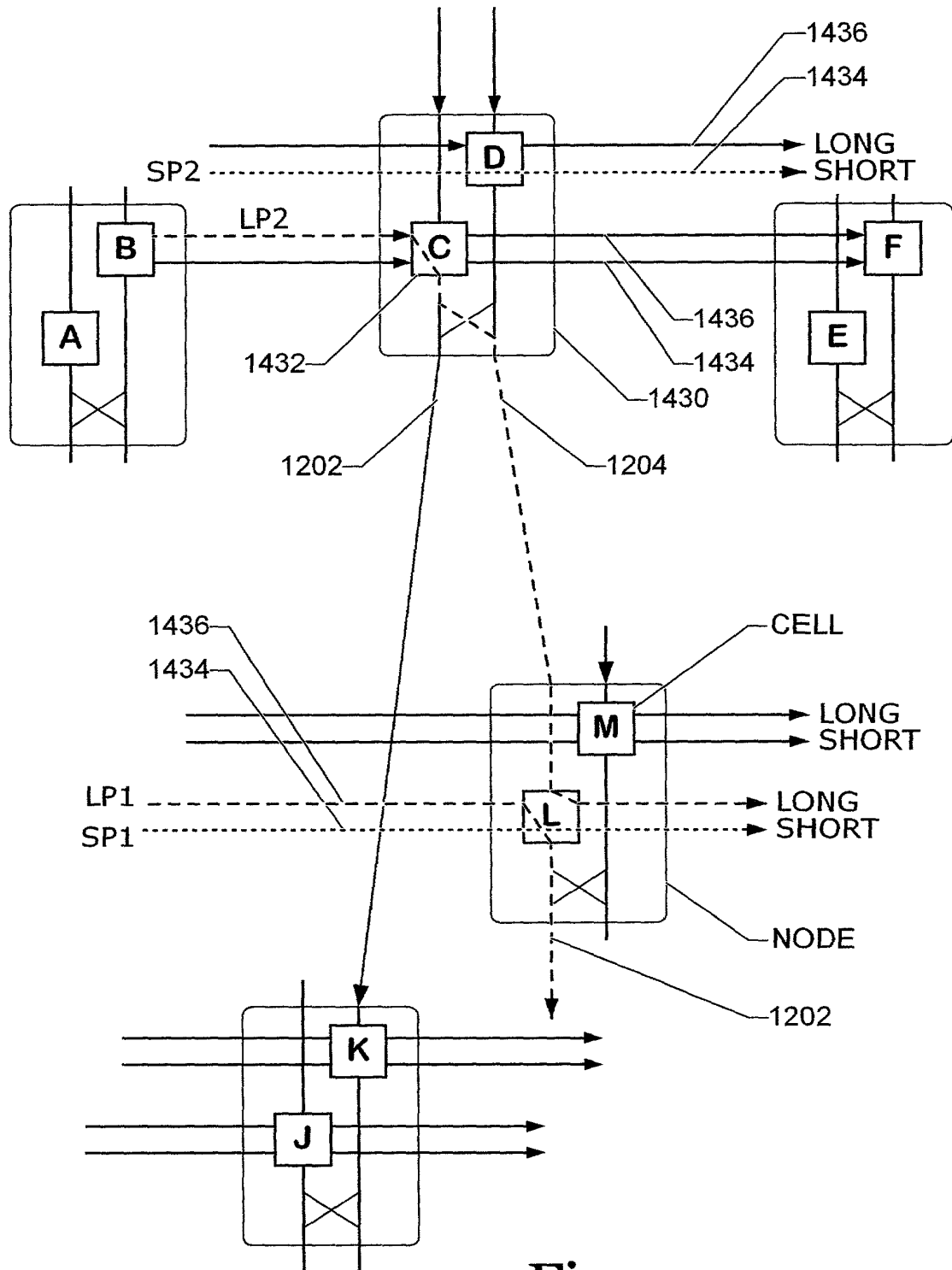


Fig 14

MULTIPLE-LENGTH SWITCH